REMARKS

This Examiner is thanked for the thorough examination of the present application. This is a full and timely response to the outstanding Office Action mailed Oct. 18, 2005. Applicant has canceled claim 1 (previously indicated as withdrawn).

The Office Action tentatively rejected all remaining claims (46-95) under 35 U.S.C. § 102(e) as allegedly being anticipated by *Tabara* (U.S. Patent 6,137,175). In reply to the Office Action, Applicant amends independent claims 46, 62, and 77 by adding a feature that "the first ILD layer is substantially flush with a top of the gate electrode." Support of these amendments can be found at least in page 9, line 15 of the original specification. Accordingly, these amendments add no new matter to the application.

Applicant respectfully requests reconsideration and withdrawal of the rejections on the grounds that the prior art of record does not disclose, teach, or suggest all of the claimed elements.

Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See e.g., In re Paulsen,* 30 F.3d 1475, 31 USPQ 2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ 2d 1655 (Fed. Cir. 1990).

Independent claim 46, as amended, recites:

> 46. A high f_{Max} deep submicron MOSFET structure, comprising:
> a substrate;
> a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode;
> a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed and ***the first ILD layer is substantially flush with a top of the gate electrode***;
> a metal gate portion:
> over the first ILD layer; and
> over the silicide portion over the gate electrode;

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the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

(*Emphasis added*).

Independent claim 46 is allowable for at least the reason that *Tabara* does not disclose, teach, or suggest the features that are highlighted in claim 46 above. More specifically, the first ILD layer taught in *Tabara* is much higher than the top of the gate electrode and cannot meet the phrase "being substantially flush with" as described in current claim 46. In the Office Action, layer 48 in Fig. 15 or layer 124 in Fig. 31 of *Tabara* is indicated as the first ILD layer in claim 46. In this regard, reference is made to Fig. 15 of *Tabara*, where layer 48 has a top surface much higher than the top of the gate electrode (36B in Fig. 9) and cannot be construed as being substantially flush with the top of the gate electrode. The same analysis is also true for the layer 124 in Fig. 31 of *Tabara*, which is not substantially flush with the top of the gate electrode (G_1 or G_2 in Fig. 20). As claim 46 (as amended herein) has at least one feature not disclosed, taught, or suggested, *Tabara* does not anticipate claim 46, and the rejection should be withdrawn.

In addition, *Tabara* fails to recognize the advantages of the present application. As listed in pages 14 and 15 of the original specification, the advantages of one or more embodiments of the present application include:

1. reduced gate noise of a RF MOSFET;

2. reduced gate resistance, resulting in a high maximum oscillation frequency;

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3. a longer unit electrode; and

4. reduced parasitic capacitance between a gate and a drain.

Tabara does not discuss RF application or oscillation frequency. Nor does *Tabara* concern the length of a gate electrode and the parasitic capacitance between a gate and a drain. Thus, *Tabara* cannot anticipate claim 46 of the present application.

As independent claim 46 is allowable over the prior art of record, then its dependent claims 47-61 are allowable as a matter of law, because these dependent claims contain all features/elements/steps of their respective independent claim 46. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Independent claims 62, as amended, recites:

> 62. A high f_{Max} deep submicron MOSFET structure, comprising:
> a substrate;
> a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode; the gate electrode having a width of from about 500 to 5000 Å;
> a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed and ***the first ILD layer is substantially flush with a top of the gate electrode***;
> a metal gate portion:
> over the first ILD layer; and
> over the silicide portion over the gate electrode;
> the metal gate portion having a width of from about 500 to 8000 Å;
> a second ILD layer over the metal gate portion and the first ILD layer;
> a first metal contact through the second ILD layer contacting the metal gate portion; and
> a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;
> whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

Likewise, independent claims 77, as amended, recites:

> 77. A high f_{Max} deep submicron MOSFET structure, comprising:
> a substrate;

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a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed and ***the first ILD layer is substantially flush with a top of the gate electrode***;

a metal gate portion:

over the first ILD layer; and

over the silicide portion over the gate electrode;

the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

(*Emphasis added.*)

Similar with the analysis for the allowability of claim 46, *Tabara* fails to disclose, teach, or suggest the features that are highlighted in either claim 62 or 77 above (*i.e.*, that "the first ILD layer is substantially flush with a top of the gate electrode"), and *Tabara* also fails to recognize the advantages of the embodiments of the present application (as discussed above). Therefore, *Tabara* cannot properly anticipate claim 62 or 77 (as amended) and the rejections should be withdrawn.

As independent claims 62 and 77 are allowable over the prior art of record, then their dependent claims 63-76 and 78-95 are allowable as a matter of law, because these dependent claims contain all features/elements/steps of their respective independent claim 62 or 77. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

In accordance with the amendments and argument in this response, the presently-outstanding rejection should be withdrawn and all pending claims allowed.

Should the Examiner have any questions regarding this response, the Examiner is invited to telephone the undersigned attorney at (770) 933-9500.

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No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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